QPI INTERCONNECT IP

The Intel® QPI protocol provides a low-latency, high-bandwidth serial link for processor-to-processor communications.

Now Users can enhance their Intel Processors and extend their servers capabilities.

Pactron's V series QPI Software Development Platforms

Intel® Quick Assist Technology:

Intel® Quick Assist Technology is a comprehensive initiative to simplify the use and deployment of accelerators on Intel® architecture platforms. This enables FPGA and Module vendors to support QPI attached in-socket acceleration hardware modules, prototyping and emulation usages. Intel® Quick Assist Technology is licensed to select vendors and consists of: QPI Referenced RTL, Software and Applications, Simulation Environment, and Validation Environment.

Pactron Vigor QPI Development System:

The Pactron V series QPI Software Development Platforms (SDP) are a complete QPI validation environment. It consist of an Intel® Xeon based server, Pactron's in-socket QPI-FPGA Accelerator Hardware Module (AHM), Intel® Quick Assist Technology and Altera OpenCL

Pactron is a QPI licensee; Pactron can provide all Intel licensed QPI and Intel® Quick Assist Technology with their products through end user license agreement. This allows users simplified accelerator integration and development paths to accelerate design productivity for Medical, High Frequency Trading (HFT), Defense, ASIC development, and other Data center applications.

The Pactron QPI-FPGA AHM can connect to the rest of the platform in 2 different configurations; Caching Agent (CA) and HA only with on-chip RAM. These configurations are ideal for designers of low-latency, signal-processing, packet processing and embedded applications, such as high-frequency trading and big data that need higher computation performance-per-watt than traditional CPU configurations can deliver.

Caching Agent allows access to system memory coherently and has a built in FPGA cache. This is excellent for accelerators that work as a co-processor, i.e., shared memory model. It is also excellent for low latency applications such as for the financial services.

3000 Patrick Henry Dr, Santa Clara, Ca 95054 408.329.5500

QPI Subsystem

Communication between the QPI subsystem of the QPI FPGA Module and the System (CPU) happens through the QPI link between the QPI FPGA Module (plugged into a CPU socket) and an adjacent CPU. As shown in Figure 1, the QPI stack can communicate over a Full-width QPI link running at 6.4GT/s with dedicated transmit and receive differential data lanes and corresponding forwarded clocks. In the future the QPI stack will support full-width link running at 8.0GT/s. There are 2 separate QPI configurations.

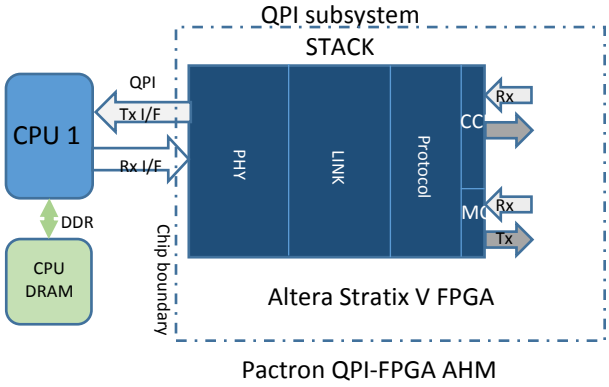


Figure 1: QPI Subsystem

Caching Agent:

Caching agent configuration, Figure 2, allows users to use accelerators to offload tasks from CPU to the FPGA AFU (accelerator function unit). The AFU can read the data from system memory, perform computations and write the results back to the system memory. The AFU is the user logic IP in which users incorporate their application specific algorithms.

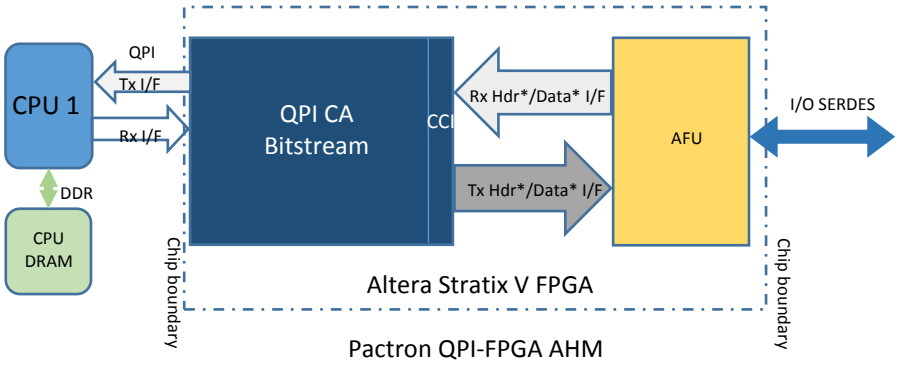
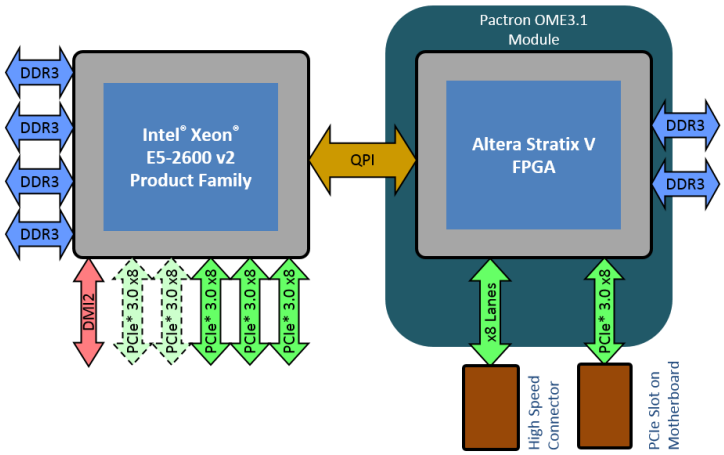


Figure 2. Caching Agent

Pactron V series QPI Software Development Platforms:

Pactron "Romley" Ivy Bridge QPI SDP

Software Development for Accelerating Workloads using Xeon and coherently attached FPGA in-socket

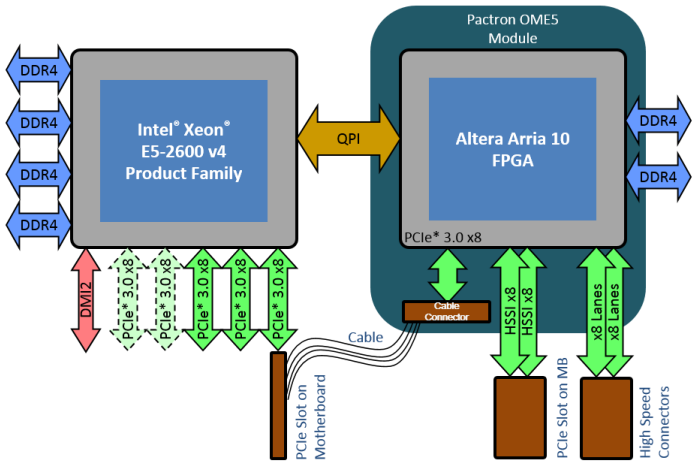


Processor	Intel® Xeon® E5-26xx v2 Processor
FPGA Module	Pactron OME3.1
QPI Speed	6.4 GT/s full width (target 8.0 GT/s at full width)
Memory to FPGA Module	2 channels of DDR3 (up to 64 GB)
Expansion connector to FPGA Module	PCIe 3.0 x8 lanes - maybe used for direct I/O e.g. Ethernet
Features	Configuration Agent, Caching Agent,, (optional) Memory Controller
Software	Accelerator Abstraction Layer (AAL) runtime, drivers, sample applications

Released and Shipping today

Pactron "Grantley" HSX/BSX QPI SDP

Software Development for Accelerating Workloads using Xeon and coherently attached FPGA in-socket



Processor	Intel® Xeon® E5-26xx v4 Processor
FPGA Module	Pactron OME5
QPI Speed	6.4 GT/s full width (target 8.0 GT/s at full width)
Memory to FPGA Module	2 channels of DDR4 (up to 64 GB)
Expansion connector to FPGA Module	Two x8 HSSI lanes (PCIe electrical) - maybe used for direct I/O e.g. Ethernet
Control Port	PCIe 3.0 x8 connected to cable connector on module. For discovery/enumeration only, not for bulk data.
Features	Configuration Agent, Caching Agent,, (optional) Memory Controller
Software	Accelerator Abstraction Layer (AAL) runtime, drivers, sample applications

** Available Dec 2015 **

Summary:

In summary, QPI is the ONLY way to connect to an Intel® server processor coherently. Now programmers can extend the flexible shared memory model that Intel® uses for x86 programming to include applications running on the Altera Stratix V or Arria 10FPGA's. Developers now have a platform environment to develop their unique accelerator applications using a Pactron V series QPI Software Development Platform.

Pactron's Design Services

Pactron customers can accelerate design productivity for QPI and other Applications by taking advantage of the design services offered by Pactron and its partners.

Pactron is a provider of Electronic Design & Manufacturing Services, supporting clients across a broad range of industry segments. Pactron designs and develops comprehensive and robust embedded systems that provide storage, wireless, mobile, networked, audio video, and Internet-connectivity for OEM markets. Pactron delivers integrated hardware and software platforms that are incorporated into end to end solutions, providing its customers minimized risk, accelerated time-to-market, reduced development costs, and enhanced design architecture.

For additional information, please send email to doug_brown@pactroninc.com, 408.329.5508